CLAIMS

1. An active matrix structure for display screen, formed on a transparent substrate, comprising pixel electrodes (P) arranged in rows and columns, a switching device associated with each electrode, and corresponding row selection lines, each selection line (L_n) being disposed between two rows of successive pixel electrodes (R_{n-1}, R_n), characterized in that it comprises under each row (R_n) of pixel electrodes, a bus (B_n) made of conducting and transparent material, substantially the same width as said row, produced on a level of the structure separated from the level of the selection lines (L_n) and from the level of the pixel electrodes (P) by at least one insulation layer and connected to the selection line (L_{n-1}) of a previous row of pixel electrodes, said bus forming a storage capacitor (Cst) with each pixel electrode of said row.

2. The active matrix structure as claimed in claim 1, characterized in that each storage capacitor bus (B_n) is connected to a previous row selection line (L_{n-1}) outside an active zone (ZA) of the matrix, at at least one end (e1).

3. The active matrix structure as claimed in claim 2, characterized in that each storage capacitor bus is connected at its two ends (e1, e2) to said previous row selection line, outside the active zone.

4. The active matrix structure as claimed in claim 1, 2 or 3, characterized in that each storage capacitor bus is connected to said row selection line at the level (e3) of each pixel element of the associated row.

5. The active matrix structure as claimed in any one of the previous claims, characterized in that the switching devices are transistors (T), the selection

line of a row (R_n) forming gate (g1) for each of the transistors of this row.

6. The active matrix structure as claimed in claim 5, characterized in that the channel level (c) of the transistors is situated between the level of the storage capacitor bus (B_n) and that of the row selection lines forming gate (g1) of the transistors (T) and in that for each transistor of a row, a portion at least of the storage capacitor bus (B_{n+1}) of the following row overlaps the channel of the transistor, said portion of bus operating as a second gate (g2) for said transistor.

7. The active matrix structure as claimed in claim 5, characterized in that the channel level (c) of the transistors is situated between the level of the storage capacitor bus (B_n) and that of the row selection lines forming gate (g1) of the transistors (T) and in that for each transistor of a row, a portion at least of the storage capacitor bus (B_n) of the row overlaps the channel of the transistor, said portion of bus operating as a second gate (g2) for said transistor.

8. The active matrix structure as claimed in claim 7, characterized in that the storage capacitor bus (B_n) of a row (R_n) of rank n in the matrix is connected to a previous row selection line, the rank of said previous row being determined as a function of the mode of addressing of the display screen in which the matrix must operate.

9. The active matrix structure as claimed in claim 8, characterized in that for a mode of addressing involving a line inversion, the storage capacitor bus of the row of rank n is connected to the selection line of the row of rank n-2.

10. The active matrix structure as claimed in claim 8, characterized in that for a mode of addressing involving a double-line inversion, the storage capacitor bus of the row of rank n is connected to the selection line of the row of rank n-4.

11. The active matrix structure as claimed in any one of claims 5 to 10, for a transistor of the type with gate below, characterized in that the storage capacitor bus is produced on a level disposed above the levels of the selection lines and the data lines.

12. The active matrix structure as claimed in any one of claims 5 to 10, for a transistor of the type with gate above, characterized in that the storage capacitor bus is produced on a level disposed below the levels of the selection lines and the data lines, directly on a substrate, or on an optical mask level.

13. A display screen comprising an active matrix structure as claimed in any one of the previous claims 1 to 12.

14. The display screen as claimed in claim 13, comprising an active matrix structure as claimed in any one of claims 5 to 12, characterized in that the row selection lines are driven by a line addressing signal of the pulse type having several voltage levels.